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Condition Monitoring for Submodule Capacitors in Modular Multilevel Converters

Hanyu Wang, *Student Member, IEEE*, Huai Wang, *Senior Member, IEEE*, Zhongxu Wang, *Student Member, IEEE*, Yi Zhang, *Student Member, IEEE*, Xuejun Pei, *Senior Member, IEEE*, and Yong Kang

***Abstract*—This letter proposes a method for the condition monitoring of submodule capacitors in modular multilevel converters (MMCs) without additional circuitry or computationally heavy algorithm. The proposed method leverages the discharging curve of submodule capacitors in connection with its parallel bleeding resistors. It is independent of the MMC control and modulation schemes. Moreover, it potentially does not require thermal and load related calibration for capacitor degradation monitoring. The principle, case study, and proof-of-concept of the proposed method are presented.**

***Index Terms*—Condition monitoring, modular multilevel converter (MMC), capacitor, discharging, reliability.**

I. Introduction

Modular multilevel converters (MMCs) have been extensively adopted in high-voltage high-power applications [1]-[3]. Many challenges exist in different aspects of MMC, such as topology [4], modulation [5], control [6], and voltage balancing [7]. However, in the critical applications, reliability should be given enough attention [8]. In the MMC-based high voltage direct current (HVDC) transmission project, hundreds of metallized polypropylene film capacitors (MPPFs) are utilized. In [9], the end-of-life (EOL) of MPPFs is typically selected as 2% to 5% capacitance reduction. After that, the capacitance will drop rapidly, leading to the waveform distortion or even collapse of the whole system. Therefore, it highly demands to develop condition monitoring (CM) techniques for submodule (SM) capacitors in the MMC to avoid unscheduled maintenance or severe failures.

Existing CM solutions for capacitor are well summarized in [10]. The first type of methods requires extra hardware circuits. However, due to the large amount of SMs and the high-voltage rating, the cost and isolation design are very challenging for the MMC. Hence, algorithm-based solutions are adopted in the MMCs [14]-[17]. In [14], a controlled AC current is injected into the circulating current for capacitance estimation. Kalman filter (KF) algorithm is used in [15] without any signal injection. In [16], the relationship between the arm average capacitance and capacitance in each SM is revealed with a simple algorithm. To simplify the calculation, a reference submodule (RSM)-based capacitor monitoring strategy is given in [17]. However, all above methods need to calculate the capacitor current based on the switching state and the measured arm current, then use the integral calculation to get the capacitance. The computational burden is quite heavy. Moreover, the accuracy is limited by the arm current ripple and the resolution of current sensor.

To avoid the interference from the main circuit, it is an effective way to achieve the CM during the shut-down period [18]-[20]. The capacitance and ESR could be acquired during the shut-down period via a variable electrical network (VEN). However, two more switches in the VEN will introduce extra unreliability problem, and increase the system cost as well [18]. The special discharging current controller [19] and complicated curve fitting algorithm [20] make it less attractive to MMC due to the high number of SMs. Besides, in MMC-based HVDC projects, the long-term uninterruptable operation is the top priority. Hence, to avoid huge economic loss, a frequent stoppage is not allowed in practical MMC applications.

To address the above limitations, in this paper, a new online CM concept for SM capacitors of MMC is proposed without the need of either switching state or arm current information. By taking full advantages of the internal *RC* discharging circuit, the health state of SM capacitors could be monitored without complicated algorithms or extra hardware circuits. Its principle and main implementation steps are illustrated in Section II. Some practical considerations are discussed in Section III. The experimental verification is given in Section IV, followed by the conclusions.

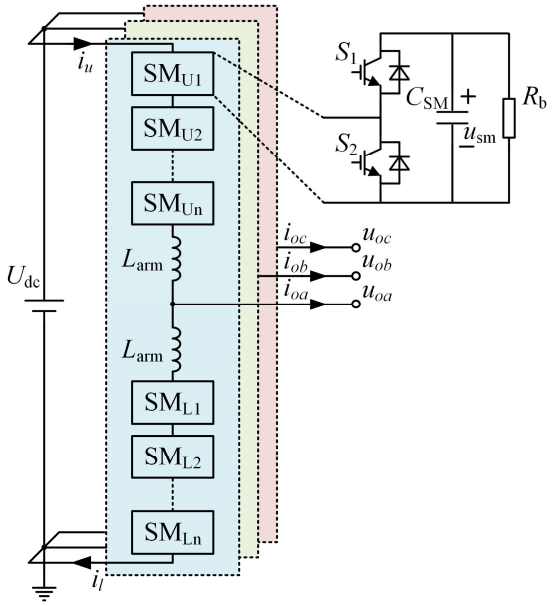

Fig. 1. Circuit configuration of a typical three-phase MMC.

H. Wang, X. Pei, and Y. Kang are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (email: wanghanyu@hust.edu.cn; ppei215@mail.hust.edu.cn; ykang@mail.hust.edu.cn).

H. Wang, Z. Wang, and Y. Zhang are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (email: hwa@et.aau.dk; zho@et.aau.dk; yiz@et.aau.dk).

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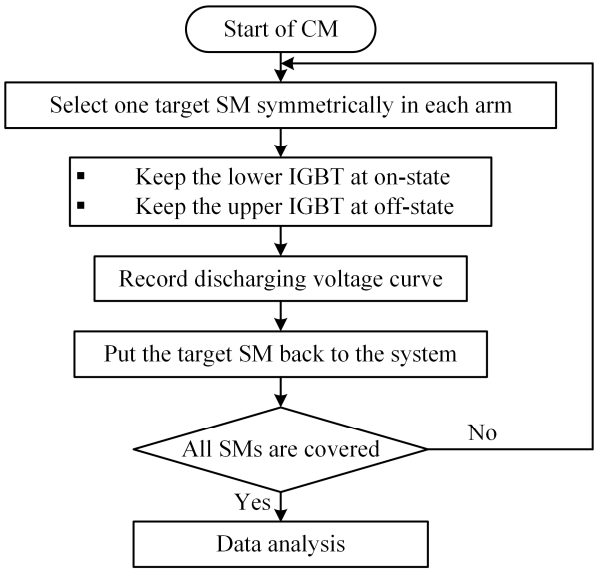


Fig. 2. Flowchart of the proposed CM method.

II. Principle and Main Steps of Proposed Online Condition Monitoring Method

A three-phase MMC, as shown in Fig. 1, has six arms, and each arm consists of N SMs and one arm inductor L_{arm}. For each SM, the half-bridge topology is the most representative one. It contains two IGBTs (S_1 and S_2) with anti-parallel diodes, a SM capacitor C_{SM}, and a bleeding resistor R_b. R_b is used to dissipate the energy stored in capacitor when the SM is shut down.

To avoid the disturbances from the main circuit during CM, the principal is to isolate the monitored SM from the system and use the discharging curve of capacitor voltage u_{sm} to get the health state.

The flowchart of the whole process is given in Fig. 2. When the CM begins, one target SM is selected symmetrically in each arm and phase. For each target SM, as shown in Fig. 3(a), the lower switch S_2 is kept at on-state, while the upper one S_1 is kept at off-state. The arm current i_{arm} flows through S_2. The SM capacitor C_{SM} is, therefore, decoupled from the main circuit, and its energy only dissipates through R_b. The discharging curve is sampled by the existing voltage sensor. For the rest SMs, they are operating as usual with some small changes in the corresponding control part.

Considering the general equivalent model of capacitor, the detailed discharging circuit is given in Fig. 3(b), where C, L_s, R_s, and R_p are the capacitance, equivalent series inductance (ESL), equivalent series resistance (ESR), and insulation resistance, respectively. The impact of ESL is negligible and not considered since its value is quite small and there is no high frequency current during the process of CM. Then, the terminal voltage across R_b is

$$u_{sm} = u_c \cdot \frac{r}{R_s + r} = U_{c\_0} e^{-\frac{t}{(R_s+r)C}} \cdot \frac{r}{R_s + r} = U_{sm\_0} e^{-\frac{t}{(R_s+r)C}} \quad (1)$$

where u_c is the voltage of C, U_{c_0} is the initial value of u_c, r is $R_p \cdot R_b/(R_p+R_b)$, and U_{sm_0} is the initial value of u_{sm}.

The discharging time t is

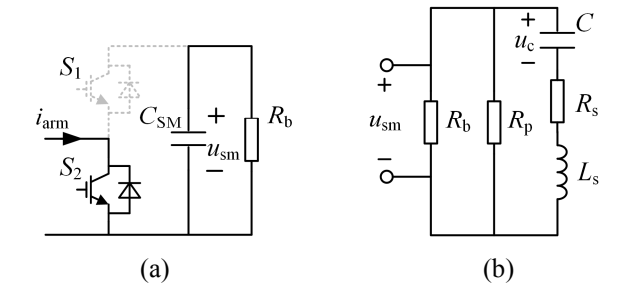
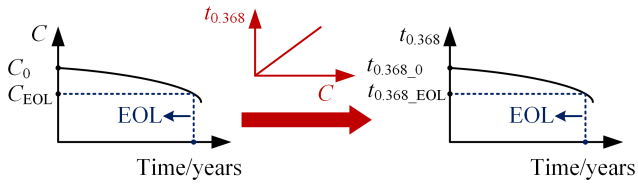


Fig. 3. Key circuit during CM. (a) Operation mode for creating RC discharging circuit. (b) Equivalent model of discharging circuit.



EOL: End-Of-Life
C_0: Initial capacitance
C_{EOL}: Capacitance at EOL
$t_{0.368\_0}$: Initial $t_{0.368}$
$t_{0.368\_EOL}$: $t_{0.368}$ at EOL

Fig. 4. Translation of degradation criteria.

$$t = (R_s + r) C \cdot \ln \frac{U_{sm\_0}}{u_{sm}}. \quad (2)$$

When u_{sm} drops to $0.368U_{sm\_0}$, equation (2) could be further simplified as

$$t_{0.368} = (R_s + r) C \quad (3)$$

where $t_{0.368}$ is the discharging time that u_{sm} drops from U_{sm_0} to $0.368U_{sm\_0}$. It is decided by R_s, r, and C, and the effect could be evaluated as

$$\begin{cases} \dfrac{\partial t_{0.368}}{\partial C} = R_s + \dfrac{R_p R_b}{R_p + R_b} \approx R_b \\ \dfrac{\partial t_{0.368}}{\partial r} = \dfrac{\partial t_{0.368}}{\partial R_s} = C. \end{cases} \quad (4)$$

Normally, R_p is at megaohm level, R_b is at kiloohm level, R_s is tens of milliohms, and C is at millifarad level. Hence, $t_{0.368}$ is dominated by the capacitance C, and almost not affected by ESR, R_p, and R_b. Equation (4) reveals the linear relationship between $t_{0.368}$ and C. Hence, the degradation of capacitor could be translated into the decrease of $t_{0.368}$, as shown in Fig. 4.

When the u_{sm} drops just below $0.368U_{sm\_0}$, the target SM in each arm could be put back into the system symmetrically. When this transition is over, the same process repeats until all other SMs are covered to complete one round of CM. Since the CM is for the long-term operation, the data analysis could be done after the information of all SMs is collected.

Unlike the existing methods [18]-[20], which have focused on calculating the value of capacitance directly during the shut-down period, the proposed method uses the discharging time to trace the degradation trend indirectly during its whole lifecycle while the system is operating. By doing the CM regularly, the health state of capacitor could be better judged with more discharging data.

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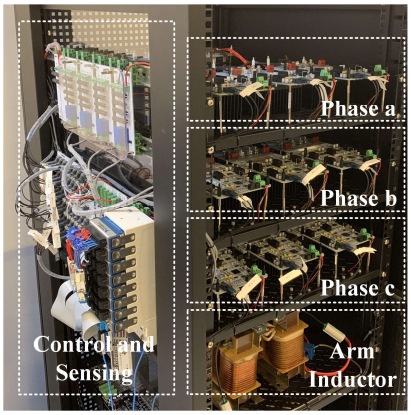

Fig. 5. Prototype of a three-phase MMC and its parameters.

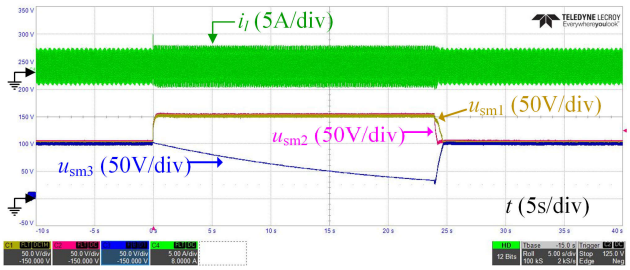

Fig. 6. Bypassing and restoration of one target SM during CM.

III. Practical Considerations of The Proposed Method

Several practical issues should be taken into account when implementing the proposed CM.

The impact on the normal operation during CM is evaluated first. The electrical stress for the rest SMs surely becomes higher after one SM is bypassed in each arm. However, in real applications, there are redundant SMs arranged in each arm [21]. For the enough design margin, the overall safety is not threatened by the absence of one SM. Besides, a symmetrical way of bypassing and restoration is adopted, and complicated control strategies for unsymmetrical situations are avoided [22]-[24]. Also, the impact on the output voltage and current during these transitions is quite small when the SM number is high. It should be noted that the discharging and charging process during the CM will not introduce any unreliability problem to the capacitor. The discharging current is very small due to the large bleeding resistor. The charging current is the arm current, which also flows through the SM in normal operation. The frequency of CM is only once a week or month, which is too low to cause accelerated ageing risk.

Due to the temperature-dependent property of capacitor and resistor, the impact of power loading and ambient temperature change should be considered. First, the arm current does not go through the capacitor or resistor during CM, avoiding the thermal impact of the power loading. Besides, the thermal impact during discharging is negligible for the large resistance of R_b and the small current. Hence, the accuracy is mainly affected by the ambient temperature, which varies in a limited range. From repetitive tests, a cluster of points are acquired, and they also appear in a limited range. The degradation is defined from the changing trend instead of a single point. In this way, temperature-related calibration is unnecessary.

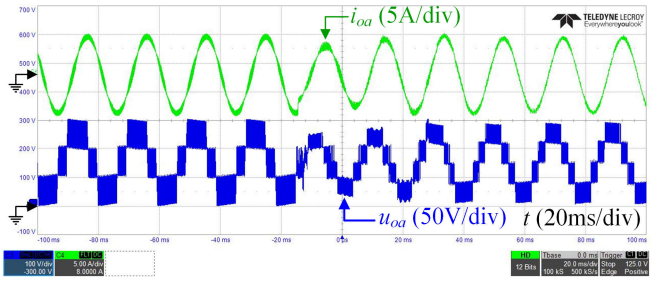

Fig. 7. The transition of output voltage and current when one SM is bypassed.

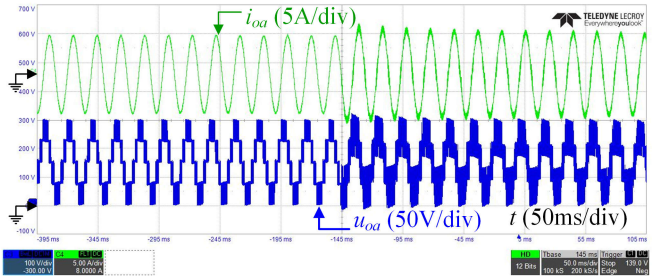

Fig. 8. The transition of output voltage and current when one SM is restored.

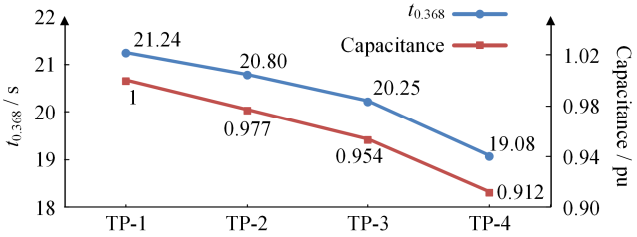

Fig. 9. Discharging time under different capacitances.

As for the measurement accuracy, it could be affected by the uncertainties from the environment and measurement. Although the interference from the main circuit has been excluded, these uncertainties still affect the result. However, this could be improved by repeating the test regularly. The timing of each CM process could be controlled at a same temperature range. In the post data processing, digital filters could be used to further improve the accuracy, and some points that deviate too much from other points are excluded in advance. Besides, the resolution of analog-to-digital converter for most digital processors is 12-bit, which is accurate enough to distinguish the 2% to 5% capacitance reduction.

Regarding the required time for one round of CM, it is mainly determined by the discharging process, which is about one RC time constant. Supposing R_b is 20 kΩ, C_{SM} is 4.5 mF, and SM number N is 100, then it takes about 2.5 hours to complete one round of CM. It is sufficient enough to enable a weekly or monthly CM.

The energy loss ΔE for each target SM during CM is

$$\Delta E = \frac{1}{2}C_{SM}U_{sm\_0}^2 - \frac{1}{2}C_{SM}(0.368U_{sm\_0})^2 = 0.43C_{SM}U_{sm\_0}^2. \quad (5)$$

The total energy loss for one round of CM is $6N{\cdot}\Delta E$. Although the most part of the stored energy in the capacitor is lost, the CM is only done once a week or month, and the efficiency in the long-term is not affected. As the price for achieving reliable

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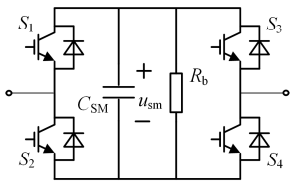
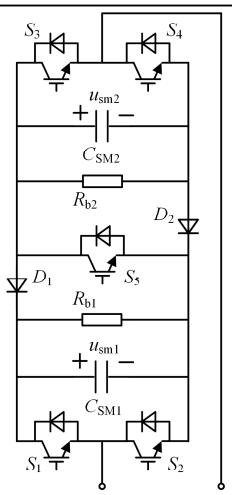
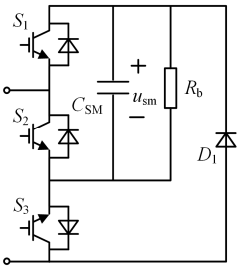
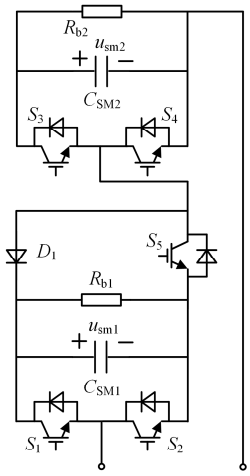
TABLE I
IMPLEMENTATION OF THE PROPOSED CM METHOD IN TYPICAL SM TOPOLOGIES

	FBSM	CDSM	CSSM	IHSM
SM Topology				
Switching State during CM	▪ Keep S_2 and S_4 at on-state ▪ Keep S_1 and S_3 at off-state ▪ Keep S_2 and S_4 at off-state ▪ Keep S_1 and S_3 at on-state	▪ Keep S_2, S_3, and S_5 at on-state ▪ Keep S_1 and S_4 at off-state	▪ Keep S_2 and S_3 at on-state ▪ Keep S_1 at off-state	▪ Keep S_2, S_4, and S_5 at on-state ▪ Keep S_1 and S_3 at off-state

online CM for hundreds of SM capacitors, this energy loss in a short time is acceptable in real project.

The proposed method works well in other SM topologies. Different SM topologies have been well summarized in [25]-[27], and some representative ones are studied here, which are full-bridge SM (FBSM), clamp double SM (CDSM), clamp single SM (CSSM), and improved hybrid SM (IHSM). The key part of CM flowchart is how to establish a *RC* discharging circuit. The implementation detail for different topologies is concluded in Table I.

IV. EXPERIMENTAL VERIFICATION

As shown in Fig. 5, a three-phase MMC prototype is built to verify the proposed method. The phase-shifted carrier (PSC) modulation is used, and the overall control strategy is the same with [6]. The sampling frequency for the capacitor voltage is 2 kHz, which is close to that in practical project [28].

The key waveforms of the lower arm in phase a are shown in Fig. 6. The third SM is selected as the target SM. After it is bypassed, its capacitor voltage u_{sm3} decreases, while the other two capacitor voltages u_{sm1} and u_{sm2} increase. The capacitor voltage reference is modified to guarantee the voltage balancing. When the discharging is over, the target SM in each arm is activated again and charged by the circulating current symmetrically. These target SMs are controllable during this period since the voltage remaining on the capacitor when discharging is over is still enough to support the auxiliary power supply. Therefore, the voltage balancing is achieved after a very short transition. Fig. 7 and Fig. 8 show the impact of CM on the output side. Without any extra control for transition, the output of the system is stable.

Fig. 9 shows the health indicator $t_{0.368}$ under different capacitances. Three smaller capacitances are used to emulate the degradation, and the discharging time is recorded under four testing points (TPs). It is proved that the small reduction of capacitance is identified accurately from $t_{0.368}$, and the degradation trend could be demonstrated clearly from the data.

V. CONCLUSION

To improve the reliability of MMC, an online CM method for SM capacitor is proposed in this paper. The main advantages of the method are summarized as below:

1) No extra sensors or circuit are needed;
2) The computational burden is reduced without the multiplication and integral operation;
3) It is convenient to repeat this CM regularly to mitigate disturbances and get the degradation trend;
4) The impact on the normal operation of MMC is negligible with the increasing number of SMs;
5) It is independent of control, modulation and loading conditions, and applicable in different SM topologies.

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